Release notes: PCA\_Rev1P0 23march2015.

1. Control processor is using SDRAM. SDRAM is going to be out dated soon as current trend to use DDR2 and DDR3. There will not be a much of support for SDRAM going forward. Control processor that is used supports only SDRAM. To use DDR3 control processor to be enhanced. Enhancing/ moving to high end control processor may be a over kill for solution/ product.
2. R-S FCC chip is interfaced using GPIO as data and address bus. This is proven and used for many applications from TI.
3. SHDSL datasheet is not available yet, this section is terminated with a header. We are expecting the datasheet to be available in a week time. We will update the design before going in to PCB.
4. Keypad interface is extended to a connector for easy of interface.
5. Control processor cannot support boot from parallel bus device. OTP devices are available in parallel bus only. There are no OTP devices available in SPI or I2C. So having very limited OTP in NOR Flash should be used at the time of booting to validate right checksum…
6. UART for RS232/ Rs422 is interface from Keystone processor GPIO due to lack of UART ports. By the way, this is proven concept in industry.
7. VOCODER is connected over UART to Keystone processor.
8. Control processor pin functionality is conflicting for SDRAM and Ethernet interface for Two pins V5 and V17. However TI is confirmed that we can use software multiplexing between two features. However further review may lead into change MII interface between FPGA to Control processer as SPI. This is under discussions with TI.
9. Majority of the parts are selected from industrial grade, the list will be release soon with comment for Industrial or Mil grade.
10. Too many components are added to meet all Keystone, FPGA, Control Processor and other peripherals requirements. May be a big challenge for board design to meet dimensions to fit all parts.